REMARKS

Present Status of the Application

The Office has rejected claims 14-15 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA) in view of Lebowitz (US 4,694,561, hereinafter "Lebowitz") in the Office Action mailed on July 11, 2005.

Applicants respectfully traverse the rejections addressed to claims 14-15 and 20-21 for at least the reasons set forth below. After carefully considering the remarks set forth in this Office Action and the cited references, Applicants respectfully submit that the presently pending claims are in condition for allowance. Reconsideration and withdrawal of the Examiner's rejection are requested.

Response to 35 USC 103 Rejection

The Office Action has rejected claims 14-15 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lebowitz (US 4,694,561, hereinafter "Lebowitz").

Applicants respectfully traverse the above rejections as set forth below.

The present invention, as basically recited in claim 14, teaches the following: "....removing a portion of the first type ion-doped well to form at least one first opening without exposing the

first type ion-doped buried layer; and forming a second type ion-doped region in the first type ion-doped well at the bottom of the first opening".

The Office alleges that Lebowitz teaches the trench capacitor, and it is thus obvious to one of ordinary skill in the art to modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz. Applicants respectfully disagree with the Office's assertion based on the following traversing:

ARGUMENT # 1

"The reason, suggestion, or motivation to combine [prior art references] may be found explicitly or implicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to references relating to possible solutions to that problem.'" Ruiz v. A.B. Chance Co., 234 F.3d 654, 665 (Fed. Cir. 2000) (quoting Pro-Mold, 75 F.3d at 1572).

"Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." Dembiczak, 175 F.3d at 999; see also Ruiz, 234 F.3d at 665.

This is because "[c]ombining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight." Dembiczak, 175 F.3d at 999.

Therefore, the federal circuit court had consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the **particular manner claimed**. See, e.g., In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000)

"Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."; In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998)

"In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

The Examiner has rejected claim 14 of the present invention on obviousness grounds without making "finding[s] as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge of [the] invention to make the combination in the manner claimed." Kotzab, 217 F.3d at 1371.

Under the United States case law, whether based on the nature of the problem to be solved, the express teachings of the prior art, or the knowledge of one of ordinary skill in the art, it is required to make specific findings as to whether there was a suggestion or motivation to combine the teachings of Lebowitz with the variable capacitor as disclosed by AAPA in the particular manner claimed by claim 14 of the present invention. See Kotzab, 217 F.3d at 1371; Rouffet, 149 F.3d at 1357.

That is, the Office was required to make specific findings as to a suggestion or motivation to modify the variable capacitor as disclosed by AAPA to form the capacitor in the bottom of an opening as taught by Lebowitz.

The obviousness test requires that the nature of the problem to be solved be such that it would have led a person of ordinary skill in the art to combine the prior art teachings in the particular manner claimed. See Rouffet, 149 F.3d at 1357. It is evident that Lebowitz does not address the same problem as the present invention. The problem to be solved of the present invention is to provide a high-frequency variable capacitor having a considerably smaller resistance occupying a smaller space. Lebowitz, on the other hand, is directed at providing a method for fabricating a VLSI DRAM array of the type whose memory cells include Hi-C trench capacitors as described in col. 2, lines 13-18 Lebowitz.

ARGUMENT # 2

The KEY question at hand is whether a person skilled in the art when faced with the problem of providing a variable capacitor having a considerably smaller resistance occupying a smaller space would be obvious to select AAPA and Lebowitz, **and** to modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz based upon the know-how during the time that the invention was made?

To try to answer the above KEY question, we have accomplished the following:

Using keywords such as "variable capacitor", "improved resistance", "Q", and "small space", "quality factor", and "high-frequency" together as well as various obvious variants of the aforementioned keywords (which are consistent with the objective of the present invention), searches were conducted using the USPTO Published Applications (AppFT), Issued Patents (PatFT) system, and the internet. The following are the search results:

Search Results using Google

1. http://www-bsac.eecs.berkeley.edu/archive/masters/patrick_riehl_ms.pdf [Micromachining of MEMS devices for producing variable capacitor that uses a vertical resonator]
2. http://www.eng.yale.edu/qlab/papers/reprints/JS_supercurrent.pdf

[Capacitor made using plates made of Au, resistors of an AuCu alloy, and Al-AlOx-Al Josephson junctions] 1999

3. http://mems.colorado.edu/c1.gen.prjct/DARPA_fame/

[Chemical approach for improving properties of ferroelectric materials. And physical approach to control the gap or area of the dielectric layer via MEMS]

4. http://kabuki.eecs.berkeley.edu/~gabed/245finalreport.pdf

[MEMS – tunable parallel plate air-gap capacitor and suspended movable plates MEMS typed variable capacitor]

5. http://en.wikipedia.org/wiki/Practical_capacitors#Variable_capacitors

[Improving via large junction area and doping profile]

USPTO Published Applications (AppFT) and Issued Patents (PatFT) search results

1. US – 2002/0040991

[Using metal-to-metal capacitors]

2. US – 2002/0158717

[Semiconductor varactor is typically noisy and lossy, particularly in applications above 500 MHz, it is ineffective for high-frequency, low-loss applications – this reference **TEACHES AWAY FROM present invention**, and suggests using Ferroelectric tunable capacitors - ceramic rare-earth oxides.]

3. US – 6,885,263

[Ferroelectric tunable capacitors - ceramic rare-earth oxides]

[Semiconductor varactor is typically noisy and lossy, particularly in applications above 500 MHz, it is ineffective for high-frequency, low-loss applications – this reference **TEACHES AWAY FROM present invention**, and suggests using Ferroelectric tunable capacitors - ceramic rare-earth oxides.]

4. US-6,806,553

[Dielectric constant is changed by application of a control voltage, and dielectric layer - a plurality of capacitance-producing regions electrically connected to each other.]

5. US -6,661,069

[Comb-drive electrodes are used for actuation while control or signal electrodes sense the motion of the movable electrode – MEMS.]

6. US-6,642,607

[Layers of different conductivities where one layer is epitaxially grown on another. A PN junction region is serving as a variable capacitance between the layers.]

Based upon the above results, it is **evident** that **the answer to the key question** of "whether a person skilled in the art when faced with the problem of providing a variable capacitor having a considerably smaller resistance occupying a smaller space for high-frequency application would be obvious to use AAPA and Lebowitz, **and to** modify the variable capacitor as disclosed by AAPA by forming the capacitor in the bottom of an opening as taught by Lebowitz based upon the know-how up to the time that the invention was made ?" **should be have been NO**.

ARGUMENT # 3

Furthermore, would there be any suggestions or teachings in Lebowitz for specifically reducing the resistance of a variable capacitor by means of modifying the variable capacitor by forming capacitor in the bottom of an opening? It seems that Lebowitz only suggested or taught mainly the following: 1) high capacitance capacitor for a DRAM, 2) direct electrical connection between capacitor and adjacent transistor, 3) a high performance DRAM cell, and 4) achieving capacitance performance in a relatively small-surface-area using a trench. [Lebowitz, Abstract, and col .1, lines 6-65]

ARGUMENT # 4

Does Lebowitz contain any teachings that **TEACHES AWAY** from the key point of contention, which is "modify variable capacitor by forming capacitor in the bottom of an opening"? The answer should be **YES** as supported in the following:

"In order to realize specified values of capacitance in relatively small-surface-area capacitors, proposals have been recently made for fabricating each cell capacitor as a vertical structure that extends into the substrate of the semiconductor chip in which the VLSI DRAM memory is formed. This so-called trench capacitor design has a major portion of its plates extending into rather than along the surface of the chip. The amount of surface area required per capacitor is only the area of the trench at the surface of the chip." [Lebowitz , Col. 31-40] In other words, Lebowitz teaches a strategy of using vertical structures in the form of trenches for achieving improved capacitance performances instead.

Based upon the above arguments/traversing, we find that there are compelling evidence which supports the patentability of claims 14-15 and 20-21 for overcoming the 35 U.S.C. 103(a) rejections based on AAPA in view of Lebowitz.

As a result, claims 14-15, and 20-21 should be allowed.

Application No.: 10/630,642 **Docket No.: JCLA8556D-R**

CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 14-27 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 12/9/2005

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809